What is claimed is:

1. A method of forming a semiconductor device with improved leakage control, comprising:

providing a semiconductor substrate having a top surface;

forming a trench in said substrate, said trench having a bottom, a first sidewall and an opposite second sidewall;

forming a leakage stop implant in said substrate under the bottom of said trench and under and aligned to said second sidewall;

filling said trench with an insulator; and

forming an N-well in said substrate adjacent to and in contact with said first sidewall, said N-well extending under said trench and forming an upper portion of an isolation junction with said leakage stop implant, said upper portion of said isolation junction located entirely under said trench.

2. The method of claim 1, further comprising forming a P-well in said substrate adjacent to and in contact with said second sidewall, said P-well incorporated into said

upper portion and forming a lower portion of said isolation junction with said N-well.

3. The method of claim 1, wherein said leakage stop implant extends under said trench from said second sidewall toward said first sidewall a distance equal to 10 to 40% of the width of said trench

4. The method of claim 1, wherein said leakage stop implant comprises P dopant and the concentration of said P dopant at an interface formed by the bottom of said trench and said substrate is 3E16 atm/cm^3 to 1E17 atm/cm^3.

5. The method of claim 4, wherein the concentration of P dopant at about 0.1 micron below said interface under said second sidewall is 1.0E17 atm/cm^3 to 1.5E17 atm/cm^3.

6. The method of claim 1, wherein said leakage stop implant is boron implanted to a dose of 2.5E12 to 5.0E12 atm/cm2 and at energies of 20 to 40 Kev.

7. The method of claim 2, further comprising forming a PFET in said N-well and an NFET in said P-well.

8. The method of claim 1, wherein said alignment of said leakage stop implant to said second sidewall of said trench is a self-alignment.

9. A method of forming a semiconductor device with improved leakage control, comprising:

providing a P doped semiconductor substrate having a top surface;

forming a trench in said substrate, said trench having a bottom, a first sidewall and an opposite second sidewall;

forming a conformal modulating layer on the top surface of said substrate and on the bottom and first and second sidewalls of said trench, said modulating layer having a outer surface;

forming a leakage stop implant in said substrate under the bottom of said trench and under and aligned to the outer surface of said modulating layer on said second sidewall;

filling said trench with an insulator; and

forming an N-well in said substrate adjacent to and in contact with said first sidewall, said N-well extending under said trench and forming an upper portion of an isolation junction with said leakage stop implant, said upper portion of said isolation junction located entirely under said trench.

10. The method of claim 9, further comprising forming a P-well in said substrate adjacent to and in contact with said second sidewall, said P-well incorporated into said upper portion and forming a lower portion of said isolation junction with said N-well.

11. The method of claim 9, wherein said leakage stop implant extends under said trench from said second sidewall toward said first sidewall a distance equal to 10 to 40% of the width of said trench

12. The method of claim 9, wherein the concentration of P dopant at an interface formed by the bottom of said trench and said substrate is 3E16 atm/cm^3 to 1E17 atm/cm^3.

13. The method of claim 12, wherein the concentration of P dopant at about 0.1 micron below said interface under said second sidewall is 1.0E17 atm/cm^3 to 1.5E17 atm/cm^3.

14. The method of claim 9, wherein said modulating layer is silicon nitride.

15. The method of claim 14, wherein said modulating layer is 40 to 80 nm thick.

16. The method of claim 9, wherein said leakage stop implant is selected from the group consisting of boron implanted to a dose of 2.5E12 to 5.0E12 atm/cm2 and at energies of 20 to 40 Kev, boron diflouride implanted to a dose of 2.5E12 to 5.0E12 atm/cm2 and at energies of 80 to 180 Kev and indium implanted to a dose of 2.5E12 to 5.0E12 atm/cm2 and at energies of 160 to 340 Kev.

17. The method of claim 10, further comprising forming a PFET in said N-well and an NFET in said P-well.

18. A semiconductor device with improved leakage control, comprising:

a P doped semiconductor substrate having a top surface;

a STI in said substrate, said STI having a bottom, a first sidewall and an opposite second sidewall;

a leakage stop implant in said substrate under the bottom of said STI and under and aligned to said second sidewall; and

an N-well in said substrate adjacent to and in contact with said first sidewall, said N-well extending under said STI and forming an upper portion of an isolation junction with said leakage stop implant, said upper portion of said isolation junction located entirely under said STI.

19. The semiconductor device of claim 18, further comprising a P-well in said substrate adjacent to and in contact with said second sidewall, said P-well incorporated into said upper portion and forming a lower portion of said isolation junction with said N-well.

20. The semiconductor device of claim 18, wherein said leakage stop implant extends under said STI from said second

sidewall toward said first sidewall a distance equal to 10 to 40% of the width of said STI

21. The semiconductor device of claim 18, wherein the concentration of P dopant at an interface formed by the bottom of said STI and said substrate is 3E16 atm/cm^3 to 1E17 atm/cm^3.

22. The semiconductor device of claim 21, wherein the concentration of P dopant at about 0.1 micron below said interface under said second sidewall is 1.0E17 atm/cm^3 to 1.5E17 atm/cm^3.

23. The semiconductor device of claim 18, further comprising spacers on said first and second sidewalls of and contained within said STI.

24. The semiconductor device of claim 23, wherein said spacers are silicon nitride.

25. The semiconductor device of claim 18, wherein said STI is filled with TEOS or HDP oxide.

26. The semiconductor device of claim 25, further including a liner on said bottom, first sidewall and second sidewall of said STI.

27. The semiconductor device of claim 26, wherein said liner is 10 to 30 nm thick thermal oxide.

28. The semiconductor device of claim 26, further comprising spacers on said liner over said first and second sidewalls of and contained within said STI

29. The semiconductor device of claim 19, wherein said STI is 0.05 to 1 micron in depth and 0.1 to 5 microns in width.

30. The semiconductor device of claim 19, further comprising a PFET in said N-well and an NFET in said P-well.

31. A method of forming a semiconductor device with improved leakage control, comprising:

providing a semiconductor substrate having a top surface;

forming a trench in said substrate, said trench having a bottom, a first sidewall and an opposite second sidewall;

forming a leakage stop implant in said substrate under the bottom of said trench and under and aligned to said second sidewall;

filling said trench with an insulator; and

forming a P-well in said substrate adjacent to and in contact with said first sidewall, said P-well extending under said trench and forming an upper portion of an isolation junction with said leakage stop implant, said upper portion of said isolation junction located entirely under said trench.

32. The method of claim 31, further comprising forming an N-well in said substrate adjacent to and in contact with said second sidewall, said N-well incorporated into said upper portion and forming a lower portion of said isolation junction with said P-well.

33. The method of claim 31, wherein said leakage stop implant extends under said trench from said second sidewall toward said first sidewall a distance equal to 10 to 40% of the width of said trench

34. The method of claim 31, wherein said leakage stop implant comprises N dopant and the concentration of said N dopant at an interface formed by the bottom of said trench and said substrate is 3E16 atm/cm^3 to 1E17 atm/cm^3.

35. The method of claim 34, wherein the concentration of N dopant at about 0.1 micron below said interface under said second sidewall is 1.0E17 atm/cm^3 to 1.5E17 atm/cm^3.

36. The method of claim 31, wherein said leakage stop implant is selected from the group consisting of phosphorous implanted to a dose of 2.5E12 to 5.0E12 atm/cm2 and at energies of 20 to 60 Kev and arsenic implanted to a dose of 2.5E12 to 5.0E12 atm/cm2 and at energies of 30 to 70 Kev.

37. The method of claim 32, further comprising forming an NFET in said P-well and a PFET in said N-well.

38. The method of claim 31, wherein said alignment of said leakage stop implant to said second sidewall of said trench is a self-alignment.

39. A method of forming a semiconductor device with improved leakage control, comprising:

providing an N doped semiconductor substrate having a top surface;

forming a trench in said substrate, said trench having a bottom, a first sidewall and an opposite second sidewall;

forming a conformal modulating layer on the top surface of said substrate and on the bottom and first and second sidewalls of said trench, said modulating layer having a outer surface;

forming a leakage stop implant in said substrate under the bottom of said trench and under and aligned to the outer surface of said modulating layer on said second sidewall;

filling said trench with an insulator; and

forming a P-well in said substrate adjacent to and in contact with said first sidewall, said P-well extending under said trench and forming an upper portion of an isolation junction with said leakage stop implant, said upper portion of said isolation junction located entirely under said trench.

40. The method of claim 39, further comprising forming an N-well in said substrate adjacent to and in contact with said second sidewall, said N-well incorporated into said upper portion and forming a lower portion of said isolation junction with said P-well.

41. The method of claim 39, wherein said leakage stop implant extends under said trench from said second sidewall toward said first sidewall a distance equal to 10 to 40% of the width of said trench

42. The method of claim 39, wherein the concentration of N dopant at an interface formed by the bottom of said trench and said substrate is 3E16 atm/cm^3 to 1E17 atm/cm^3.

43. The method of claim 42, wherein the concentration of N dopant at about 0.1 micron below said interface under said second sidewall is 1.0E17 atm/cm^3 to 1.5E17 atm/cm^3.

44. The method of claim 39, wherein said modulating layer is silicon nitride.

45. The method of claim 44, wherein said modulating layer is 40 to 80 nm thick.

46. The method of claim 39, wherein said leakage stop implant is selected from the group consisting of phosphorus implanted to a dose of 2.5E12 to 5.0E12 atm/cm2 and at energies of 20 to 60 Kev and arsenic implanted to a dose of 2.5E12 to 5.0E12 atm/cm2 and at energies of 30 to 70 Kev.

47. The method of claim 40, further comprising forming an NFET in said P-well and a PFET in said N-well.

48. A semiconductor device with improved leakage control, comprising:

an N doped semiconductor substrate having a top surface;

a STI in said substrate, said STI having a bottom, a first sidewall and an opposite second sidewall;

a leakage stop implant in said substrate under the bottom of said STI and under and aligned to said second sidewall; and

a P-well in said substrate adjacent to and in contact with said first sidewall, said P-well extending under said STI and forming an upper portion of an isolation junction with said leakage stop implant, said upper portion of said isolation junction located entirely under said STI.

49. The semiconductor device of claim 48, further comprising an N-well in said substrate adjacent to and in contact with said second sidewall, said N-well incorporated into said upper portion and forming a lower portion of said isolation junction with said P-well.

50. The semiconductor device of claim 48, wherein said leakage stop implant extends under said STI from said second sidewall toward said first sidewall a distance equal to 10 to 40% of the width of said STI

51. The semiconductor device of claim 48, wherein the concentration of N dopant at an interface formed by the bottom of said STI and said substrate is 3E16 atm/cm^3 to 1E17 atm/cm^3.

52. The semiconductor device of claim 51, wherein the concentration of N dopant at about 0.1 micron below said interface under said second sidewall is 1.0E17 atm/cm^3 to 1.5E17 atm/cm^3.

53. The semiconductor device of claim 48, further comprising spacers on said first and second sidewalls of and contained within said STI.

54. The semiconductor device of claim 53, wherein said spacers are silicon nitride.

55. The semiconductor device of claim 48, wherein said STI is filled with TEOS or HDP oxide.

56. The semiconductor device of claim 55, further including a liner on said bottom, first sidewall and second sidewall of said STI.

57. The semiconductor device of claim 56, wherein said liner is 10 to 30 nm thick thermal oxide.

58. The semiconductor device of claim 56, further comprising spacers on said liner over said first and second sidewalls of and contained within said STI

59. The semiconductor device of claim 49, wherein said STI is 0.05 to 1 micron in depth and 0.1 to 5 microns in width.

60. The semiconductor device of claim 49, further comprising an NFET in said P-well and a PFET in said N-well.